REMARKS

Claims 1-14 were pending in the application prior to the present amendment.
Claim 1 and 6 have been amended.
Thus, Claims 1-14 will be pending in the application after entry of the present amendment.

Objection to the Abstract

The Examiner objected to the Abstract of the Disclosure because of its use of legal phraseology, i.e., its use of the word "comprises". Thus, the Abstract has been amended to substitute a standard legal definition for the word "comprises", i.e., to substitute the phrase "includes, but is not necessarily limited to". Thus, no new matter has been added to the disclosure by virtue of this substitution.

Objection to the Disclosure

The Examiner objected to the Applicant's use of the term "SIMD (simultaneous-instruction multiple-data)" at line 7 of page 4 of the specification. Applicant has made an inadvertent error by using the word "simultaneous" instead of the word "single". Thus, Applicant has made an amendment to the specification to substitute the word "single" for the word "simultaneous". Applicant wishes to draw the Examiner's attention to multiple other portions of the specification where the term "SIMD" was correctly rendered as "single-instruction multiple-data" in the application as filed. Namely, please refer to (a) page 2, lines 22-23; (b) page 14, line 14; and (c) page 38, line 6. Thus, the substitution of the word "single" for the word "simultaneous" at page 4, line 7 of the specification does not constitute the addition of new matter.

Rejections under Section 112

Claims 6-14 were rejected under 35 U.S.C. Section 112, second paragraph, as being indefinite. The Examiner states that:

> "As per claim 6, the term 'two-dimensional discrete cosine' (line 4) should be --two dimensional **inverse** discrete cosine--. The terms '(2D-DCT)' and '2D-

DCT should be --(2D-IDCT)-- and --2D-IDCT--, respectively. Similarly noted claims 7-18, 12 and 13."

Applicant respectfully traverses these rejections. It is natural for an inverse discrete cosine transform to operate on two-dimensional discrete cosine transform (2D-DCT) coefficient blocks, i.e., coefficient blocks that correspond to the two-dimensional frequency domain, e.g., coefficient blocks that are derived from a previously performed two-dimensional discrete cosine transform operation. Thus, it is not inappropriate or vague for an input interface of an inverse discrete cosine transform module to "receive two-dimensional discrete cosine transform (2D-DCT) coefficient blocks" as recited in claim 6. Thus, Applicant retains the use of the term "two-dimensional discrete cosine transform coefficient blocks" in claims 6, 8 and 12.

The term "two-dimensional discrete cosine" does not occur in claim 7. Thus, it is not apparent to the Applicant what language in claim 7 forms the basis for the Examiner's rejection of claim 7. Clarification is requested.

Rejections Under Section 103(a)

The Examiner rejected Claims 1-5 under 35 U.S.C. Section 103(a) as being unpatentable over Van Eijndhoven et al. (U.S. Patent No. 6,397,235). Applicant respectfully traverses these rejections.

Van Eijndhoven et al. discloses a data processing device and method for computing the cosine transform of a matrix. At lines 5-21 of Col. 3, Van Eijndhoven et al. teaches:

> "FIG. 1 shows a VLIW type (Very Long Instruction Word) data processing device. Although the invention is illustrated using a VLIW type device, it is not limited to such a device. The device contains an instruction issue unit 10, a number of functional units 12a-c and a register file 14. The instruction issue unit 10 has an instruction output coupled to the functional units 12a-c and the register file 14. The register file 14 has read/write ports coupled to operand inputs/outputs of the functional units 12a-c." *[Emphasis added]*
>
> "One functional unit 12a is shown in more detail. This functional unit 12a contains an instruction decoder 120, a number of ALU's (Arithmetic/Logic units) 122a-d, a first and second input register 124a,b and an output register 126. The instruction decoder is connected to the ALU's 122a-d. The input

registers 124a,b are divided into a number of segments. The segments of the first and second input registers 124a,b are connected to the ALU's 122a-d." *[Emphasis added]*

At lines 5-27 of Col. 4, Van Eijndhoven et al. discloses:

"SIMD instructions may be applied for example to compute a one dimensional transform of a number of columns of a block B of numbers $B_{i,j}$ (i=0.n, j=0.m), e.g. an 8x8 block (n=7, m=7). To do so, numbers from the same rows of the block are loaded into different segments of a register. For example, numbers $B_{0,0}$, $B_{0,1}$, $B_{0,2}$, $B_{0,3}$ are loaded into segments S0, S1, S2, S3 of a first register R1 respectively, $B_{0,4}$, $B_{0,5}$, $B_{0,6}$, $B_{0,7}$ are loaded into segments S0, S1, S2, S3 of a second register R2 respectively, $B_{1,0}$, $B_{1,1}$, $B_{1,2}$, $B_{1,3}$, are loaded into segments S0, S1, S2, S3 of a third register R3 respectively, $B_{1,4}$, $B_{1,5}$, $B_{1,6}$, $B_{1,7}$ are loaded into segments S0, S1, S2, S3 of a fourth register R4 respectively and so on." *[Emphasis added]*

"Now assume that a program is available to perform the transformation on one column, the program being expressed in instructions which include arithmetic instructions like add, subtract, multiply etc. applied to registers which contain the numbers for one column $B_{i,j}$ i=0.n. If SIMD instructions are used for all these arithmetic instructions then this program will automatically compute the transform in parallel for a number of columns j=0.3. Thus, in case of a block with N-columns and P numbers in respective segments of each register, the program would need to be executed only N/P times to transform the N columns." *[Emphasis added]*

Separable two-dimensional transformations such as the inverse discrete cosine transform may be accomplished by performing a one-dimensional transformation on each column of an input block to obtain columns of an intermediate block, and a one-dimensional transformation on each row of the intermediate block to obtain rows of an resultant block, as disclosed at Col. 4, lines 28-58, and Col. 11, lines 17-32. At lines 38-43 of Col. 5, Van Eijndhoven et al. discloses that:

"In order to be able to use SIMD instructions for both types of transformations the intermediate block needs to be transposed: the numbers have to be regrouped over the registers. This is a complicated operation: in the example of an 8x8 block with 4-segment registers one needs 16 registers and 32 operations with two-inputs for the transposition."

"The invention aims at avoiding the transposition. For the transformation of the rows the arrangement of the numbers of the intermediate block wherein registers contain different numbers from the same row is retained, and special

> instructions are used that combine these numbers from these registers in order to perform the one dimensional transformation in the row that is stored in these registers." *[Emphasis added]*
>
> "These instructions make it possible to perform a two-dimensional separable transformation without transposition. Without farther measures, the combination of such special instructions for one dimension and the SIMD type of operations for two or more further dimensions can be used to perform higher than 2 dimensional transformations as well."
>
> "In the most straightforward implementation at least one functional unit is provided that is capable of performing the entire IDCT of a row. In case of an 8-point IDCT using registers that each contain four respective numbers from a column, such an instruction would need two operand registers and two result registers." *[Empahsis added]*

In the section starting at Col. 7, line 1 and extending through Col. 10, line 22, Van Eijndhoven et al. discloses a set of instructions INS1, INS2, ..., INS7 that correspond to respective subdiagrams of the flow diagram of Figure 3. Van Eijndhoven et al. discloses functional units for executing instructions INS1 and INS2 in Figures 4b and 4a respectively. At Col. 9, lines 49-60, Van Eijndhoven et al. discloses a program written in terms of instructions INS1-INS7 that performs an 8-point IDCT of a row. In the passage starting at Col. 9, line 63 and extending through Col. 10, line 6, Van Eijndhoven et al. discloses that:

> "To transform a complete block these instructions must be repeated for the other rows, with other registers as far as necessary. Needless to say that in a VLIW processor, with more than one functional unit, although all these instructions INS1-INS7 may be instructions for the same single functional unit, it is also possible that these instructions may be executed by different functional units. For example, specialized functional units might be provided for the instructions which involve multiplication on one hand and instructions which involve only additions and subtractions on the other hand." *[Emphasis added]*

Observe that Van Eijndhoven et al. nowhere teaches or suggests:

> "... receiving multiple coefficient blocks ...; grouping together respective elements from the multiple coefficient blocks to produce one block of 2D coefficient vectors; and operating on the block of 2D coefficient vectors with SIMD instructions to carry out the 2D-IDCT on the multiple coefficient blocks"

as recited in currently amended Claim 1. While Van Eijndhoven et al. does disclose a data processing device with multiple functional units (e.g., in Figure 1), Van Eijndhoven et al. nowhere teaches or suggest that the multiple function units may be used to perform the action of "grouping together respective elements from the multiple coefficient blocks to produce one block of 2D coefficient vectors", or the action of "operating on the block of 2D coefficient vectors with SIMD instructions to carry out the 2D-IDCT on the multiple coefficient blocks" as recited in Claim 1.

Thus, Claim 1 and its dependents are patentably distinguished over Van Eijndhoven et al. at least for the reasons given above.

The Examiner stated that "It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Van Eijndhoven et al's teachings, because the reference is a data processing device/method for performing 2-D IDCT having SIMD instructions as claimed." Applicant respectfully disagrees. Van Eijndhoven et al. performs a 2D IDCT on a single input block of numbers using (a) SIMD instructions to transform columns of the input block and (b) dedicated instructions to transform rows of the intermediate block as disclosed in the following passages:

> "The invention aims at avoiding the transposition. For the transformation of the rows the arrangement of the numbers of the intermediate block wherein registers contain different numbers from the same row is retained, and special instructions are used that combine these numbers from these registers in order to perform the one dimensional transformation in the row that is stored in these registers." (Col. 5, lines 25-31).

> "Thus, the 2-dimensional IDCT transformation can be performed for the columns using arithmetic SIMD instructions to apply a one-dimensional IDCT-transformation to a number of columns in parallel and for the rows using a different, dedicated IDCT instruction to apply a functionally identical IDCT-transformation to a row." (Col. 6, lines 26-31)

None of the instructions or functional units disclosed by Van Eijndhoven et al. operate on blocks of 2D coefficient vectors, each vector containing respective elements from multiple coefficient blocks. Thus, it would not have been obvious for one skilled in the relevant art to conceive of the invention of Claim 1 from the teachings of Van Eijndhoven et al.

CONCLUSION

Applicant submits that the application is in condition for allowance, and an early notice to that effect is requested. If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant hereby petitions for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 501505/5500-59700/BNK. Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Request for Approval of Drawing Changes

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $___ for fees ( ).

☐ Other: IDS, including PTO-1449 form and cited references

Respectfully submitted,

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